REMARKS

After entry of this amendment, claims 1-5, 7-15, 17-25, and 27-55 remain pending. In the present Office Action, claims 31-41 and 52-55 were rejected under 35 U.S.C. § 101. Claims 32-33 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1, 11, 21, 31-33, and 42 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kogge, U.S. Patent No. 5,475,856 ("Kogge"). Claims 4, 14, 24, and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kogge. Claims 43-44, 48-49, and 52-53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kogge in view of Tran et al., U.S. Patent No. 6,014,734 ("Tran"). Applicants respectfully traverse these rejections, and request reconsideration. Claims 2-3, 5, 7-10, 12-13, 15, 17-20, 22-23, 25, 27-30, 45-47, and 50-51 were indicated as allowable if rewritten in independent form.

Claims 1, 4, 11, 14, 21, 24, 31-33, 36, and 42

Applicants respectfully submit that each of claims 1, 4, 11, 14, 21, 24, 31-33, 36, and 42 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "the execution core is configured to store a first address in the third register responsive to the first instruction, wherein the first address is an address of a second instruction following the first instruction".

The present Office Action alleges that the first and second registers in claim 1 are the IR 105 of processor 1 and the IR 105 of any of the other processors 2-N, respectively, when they store a branch instruction which includes target address information (see Office Action, page 5, lines 1-10). Additionally, the present Office Action alleges that the processor selects the first target address as the next program counter address in the SIMD mode and the second target address as the next program counter address in the MIMD mode responsive to a "first instruction" (see present Office Action, page 5, line 16-page 6, line 4). Accordingly, since the processors execute the branch instruction in their respective IR 105 to branch to the target address as the next program counter

address, the Office Action is asserting that the first instruction is a branch instruction in Kogge.

The Office Action then goes on to allege that the third register in claim 1 is taught by the PC 103 and to allege that "the execution core is configured to store a first address in the third register responsive to the first instruction, wherein the first address is an address of a second instruction following the first instruction" is taught by the next instruction address being saved in the PC 103 after the first instruction is executed. However, since the first instruction is alleged to be a branch instruction and the present Office Action alleges that the first or second target address is selected as the next program counter address in response to the branch instruction, the PC 103 would be storing the first or second target address after executing the branch instruction (not the address of the next instruction after the branch instruction). Accordingly, the PC 103 cannot teach or suggest the third register as recited in claim 1, wherein "the execution core is configured to store a first address in the third register responsive to the first instruction, wherein the first address is an address of a second instruction following the first instruction".

Furthermore, in the SIMD mode, Kogge teaches that the PC is not automatically incremented when an instruction is executed unless that instruction is a two word immediate instruction such as load immediate (Kogge, col. 7, lines 7-11). Thus, Kogge teaches that at least in the SIMD mode, the PC 103 does not store the address of the next instruction after an instruction is executed. In particular, branch instructions are not two word immediate instructions in Kogge and thus there is no update of the PC 103 to the next instruction in SIMD mode, contrary to the assertion in the Office Action.

For at least the above-stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 4 and 42, dependent from claim 1, are also patentable over the cited art for at least the above stated reasons as well. Claim 11 recites a combination of features including: "the processor is configured to store a first address in the third storage location responsive to the first instruction, wherein the first address is an address of a

second instruction following the first instruction". Claim 21 recites a combination of features including: "storing a first address in a third register responsive to executing the first instruction, wherein the first address is an address of a second instruction following the first instruction". Claim 31 recites a combination of features including: "store a first address in a third storage location responsive to the first instruction, wherein the first address is an address of a second instruction following the first instruction". The same teachings of Kogge highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claims 11, 21, and 31 as well. Applicants respectfully submit that Kogge does not teach or suggest the above highlighted features of claims 11, 21, and 31, either. Accordingly, claims 11, 21, and 31 are patentable over the cited art for at least the above stated reasons. Claims 14, 24, 32-33, and 36 depend from one of claims 11, 21, and 31, and thus these claims are patentable over the cited art for at least the above stated reasons as well. Each of claims 4, 14, 24, 32-33, 36, and 42 recite additional combinations of features not taught or suggested in the cited art.

Section 103 Rejection of Claims 43-44, 48-49, and 52-53

Applicants respectfully submit that each of claims 43-44, 48-49, and 52-53 recite combinations of features not taught or suggested in the cited art. For example, claim 43 recites a combination of features including: "the execution core is configured to establish, responsive to the first instruction, an operating mode in the processor for executing a *second instruction* stored at the first address, the operating mode selected from a plurality of operating modes responsive to the operand size of the *first instruction*".

The Office Action alleges that Kogge discloses the invention as set forth in claim 1 except for "the operating mode selected from a plurality of operating modes responsive to the operand size of the instruction". Applicants respectfully disagree that Kogge discloses all the other features of claim 1. Furthermore, the Office Action goes on to allege that Tran teaches the operating mode selected from a plurality of operating modes responsive to the operand size of the instruction, citing col. 19, lines 10-15. The pertinent part of these teachings is: "The first four registers, EAX, EDX, ECX, and EBX, have

operand sizes of 8, 16, or 32-bits depending on the mode of the processor or instruction." (Tran, col. 19, lines 12-15). While Tran generally teaches that instructions can have different operand sizes, nothing in this teaching describes establishing the operating mode for a second instruction responsive to the operand size of the first instruction. Rather, the instructions being described in the cited section of Tran can set the operand size of a given instruction using a prefix byte, but that operand size only affects the given instruction, not other instructions. The processor mode can also affect operand size in Tran, but that is not the same as establishing an operating mode for one instruction responsive to the operand size of another instruction. Thus, Tran does not teach or suggest the above highlighted features of claim 43. Moreover, the alleged combination of Kogge and Tran does not teach or suggest the combination of features recited in claim 43.

For at least the above stated reasons, Applicants submit that claim 43 is patentable over the cited art. Claim 44, being dependent from claim 43, is similarly patentable over the cited art for at least the above stated reasons. Claim 48 recites a combination of features including: "the processor is configured to establish, responsive to the first instruction, an operating mode in the processor for executing a second instruction stored at the first address, the operating mode selected from a plurality of operating modes responsive to the operand size of the first instruction". Claim 52 recites a combination of features including: "establish an operating mode for executing a second instruction stored at the first address, the operating mode selected from a plurality of operating modes responsive to the operand size of the first instruction". The same teachings of Tran and Kogge highlighted above with regard to claim 43 are alleged to teach the features of claims 48 and 52. Applicants respectfully submit that the alleged combination of Kogge and Tran does not teach or suggest the above highlighted features of claims 48 and 52, either. Accordingly, Applicants submit that claims 48 and 52 are patentable over the cited art. Claims 49 and 53, being dependent from claims 48 and 52, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 44, 49, and 53 recites additional combinations of features not taught or suggested in the cited art.

Section 112 Rejection

The present Office Action rejected claims 32-33 under 35 U.S.C. § 112, second paragraph as being indefinite. The Office Action alleges that it is not clear how the plurality of instructions can be executed responsive to the first instruction (as indicated in claim 31) and also emulate the first instruction (as indicated in claim 32) or be executed in place of the first instruction (as indicated in claim 33). Applicants respectfully disagree with the rejection. However, Applicants have further clarified these claims by amending claim 31 to recite "a plurality of instructions which, when executed responsive to an occurrence of a first instruction in a code sequence". Applicants respectfully submit that the amendment obviates the rejection.

Section 101 Rejection

The present Office Action alleges that claims 31-41 and 52-55 are non-statutory because the computer readable medium is allegedly defined to include intangible embodiments such as transmission media or signals. Applicants respectfully disagree. The specification defines a carrier medium to include transmission media or signals. On the other hand, claims 31-41 and 52-55 recite a *computer readable* medium *storing* a plurality of instructions. Applicants respectfully submit that the recited computer readable medium is statutory. However, merely to expedite allowance of the claims, Applicants have amended independent claims 31 and 52 to recite a tangible computer readable medium.

CONCLUSION

Applicants respectfully submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-66000/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,

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